Analogue and RF performances of Fully Depleted SOI MOSFET

Performances analogiques et RF de MOSFETs SOI complétement désertés

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RÉSUMÉ. Les performances des circuits intégrés RF sont directement liées aux caractéristiques analogiques et haute fréquence des transistors, à la qualité des interconnexions métalliques ainsi qu'aux propriétés électromagnétiques du substrat. Grâce à l'introduction sur le marché du substrat SOI (Silicium sur Isolant) à haute résistivité et riche en pièges, les spécifications des circuits intégrés en termes de linéarité sont satisfaites. Aujourd'hui, le MOSFET SOI partiellement déserté (PD) est la technologie principale des systèmes SOI RF. Les futures générations de systèmes de communication mobiles nécessiteront des transistors offrant de meilleures performances haute fréquence, fonctionnant à une consommation d'énergie inférieure et dans la plage des ondes millimétriques. Le MOSFET SOI entièrement déserté (FD) est un candidat très prometteur pour le développement de ces futurs systèmes de communication sans fil. La plupart des données rapportées sur FD SOI concernent leurs performances digitales. Dans cet article, leur comportement analogique / RF est décrit et comparé aux MOSFETs en silicium massif. Les problèmes d'auto-échauffement, le comportement non linéaire ainsi que les performances haute fréquence aux températures cryogéniques des MOSFETs FD SOI sont discutés. Enfin, un bref résumé des IC publiés aux ondes RF et millimétriques basés sur la technologie FD SOI est présenté.

ABSTRACT. Performance of RF integrated circuit (IC) is directly linked to the analogue and high frequency characteristics of the transistors, the quality of the back-end of line process as well as the electromagnetic properties of the substrate. Thanks to the introduction of the trap-rich high-resistivity Silicon-on-Insulator (SOI) substrate on the market, the ICs requirements in term of linearity are fulfilled. Today Partially Depleted (PD) SOI MOSFET is the mainstream technology for RF SOI systems. Future generations of mobile communication systems will require transistors with better high frequency performance operating at lower power consumption and in the millimeter-waves range. Fully Depleted (FD) SOI MOSFET is a quite promising candidate for the development of these future wireless communication systems. Most of the reported data on FD SOI concern their digital performance. In this paper, their analogue/RF behaviour is described and compared with bulk MOSFETs. Self-heating issue, non-linear behaviour as well as high frequency performance at cryogenic temperature for FD SOI MOSFET are discussed. Finally, a brief summary of the published RF and millimeter-waves ICs based on FD SOI technology is presented.

MOTS-CLÉS. Silicium sur Isolant (SOI), complètement déserté (FD), comportement haute fréquence, Radio Fréquence (RF), ondes millimétriques, performances analogiques et RF, auto-échauffement, comportement non-linéaire, température cryogénique, circuits intégrés (IC).

KEYWORDS. Silicon-on-Insulator (SOI), Fully Depleted (FD), high frequency behaviour, Radio Frequency (RF), millimeter-waves, analogue/RF performances, self-heating, non-linear behaviour, cryogenic temperature, Integrated Circuits (ICs).

1. Introduction

The Radio Frequency (RF) performance of an integrated circuit will not only depend on the analogue and high frequency characteristics of the active devices, i.e. the transistors, but also the quality of the back-end of line (BEOL) process which defines the losses along the interconnection line and the quality factor of the passive elements such as the inductors and tunable capacitors, as well as the electromagnetic properties of the substrate on which the RF integrated circuit (IC) is lying. Figure 1 schematically represents the three important levels of optimization for a RF IC.

The parasitic resistances (metal lines and vias) and capacitances (dielectric layers) along the interconnection constitute a low-pass filter which drastically limits the operational frequency of ICs

[CLA 14]. Advanced BEOL process provides higher number of metal lines, thicker metal layers, low-k dielectric interlayers and denser vias using carbon nanotubes are investigated for diminishing the parasitic resistances between metal layers [INO 13, TAG 11, KIN 14, WU 14, CEY 13].

The substrate losses and crosstalk remain a challenge for designing high-performance ICs in Si-based technologies for RF applications. In 1997, the RF performance of high-resistivity (HR) Silicon-on-Insulator (SOI) substrate material was presented for the first time [RAS 97]. The great potential of HR SOI substrate to reduce RF losses as well as the crosstalk in Si-based substrates was demonstrated. Prior to this work, the scientific community considered the Si-based substrate as the limiting and blocking obstacle for working RF ICs. In 2000's, Prof. Raskin's research team made the fundamental discovery that enables the success of RF-SOI on the market today. The root cause of missing RF performance of standard HR SOI was found by demonstrating the existence of a parasitic surface conduction [WU 99, LED 00, LED 03] below the buried oxide and the way to disable it by introducing traps. In 2005, the possibility of creating HR SOI substrates characterized with an effective resistivity as high as 10 kΩ.cm due to the silicon surface modification below the buried oxide (BOX) of a high resistivity SOI substrate was demonstrated [LED 05]. The surface modification consists of the introduction of a high density of defects called traps at the BOX / HR-Si handle substrate interface. There are several ways to create those traps [LED 05, GAM 99, WON 04] but the grain boundaries in a thin polysilicon layer have been shown as a quite efficient and robust solution.

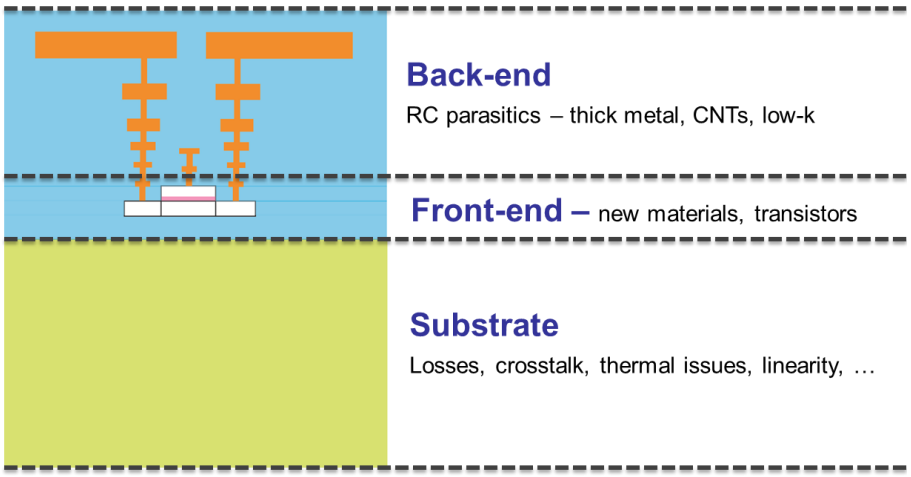


Figure 1. *RF IC quality relies on the back-end and front-end of line processes as well as the substrate electromagnetic properties.*

Today, partially depleted (PD) Silicon-on-Insulator (SOI) with a channel length of 130 nm is the mainstream technology for RF SOI ICs. New generation of mobile communication systems such as 5G require higher cutoff frequency for the system, better linearity and lower power consumption. Moreover the integration of high quality passive elements such inductors requires higher number and thicker metal layers. Thus, for getting higher transistor cutoff frequencies and better BEOL, RF SOI must move to shorter nodes. However, further reduction of device dimensions is problematic due to intrinsic physical limitations such as short channel effects, high current leakage through gate dielectrics, high series resistances, low mobility due to interface effects and high doping levels, high current density and thus self-heating and reliability issues, and so on. The most common strategies to address these challenges include the introduction of new materials such as germanium, III-V, high-k gate dielectrics and metal gates, low-k for the back-end dielectrics and gate spacers, SOI technology, strain channel engineering, and alternative device architectures such as multiple gate, i.e. FinFET, planar double-gate, gate-all-around (GAA) nanowires, or tunnel FET, etc.

Fully Depleted (FD) electronic regime is a promising approach to continue scaling of MOSFETs. Scaling the thickness of the silicon body is proposed in the case of FinFET and ultra-thin body and buried oxide (BOX), named as UTBB, technologies in order to control short channel effects (SCE)

[LIU 10, HIS 00]. In order to limit SCE, the channel thickness must be approximately 1/4 and 2/3 of the channel length, respectively, in the case of UTBB and FinFET. Technological aspects, electrostatics, scalability and variability issues in UTBB FD-SOI MOSFETs as well as their perspectives for low power digital applications are widely discussed and shown to be excellent [FEN 10a, AND 10, FEN 10b, MON 10, BUR 10, RUD 10, BUR 09, MD 12, RUD 14, MAK 14a]. However, lateral coupling of source and drain through the substrate is enhanced in the case of thin-BOX devices. To mitigate this parasitic substrate coupling a highly-doped layer is implanted right underneath the BOX, or so-called Ground Plane (GP), which screens or prevents electric field lines penetration into the substrate. Furthermore, the GP opens a practical way for multi-threshold voltage (Vth) and back-gate biasing schemes realization [MD 13].

In this paper, the analogue/RF behaviour of FD SOI transistors is described and compared with bulk MOSFETs in Section 2. Self-heating issue, non-linear behaviour as well as high frequency performance at cryogenic temperature for FD SOI MOSFET are discussed, respectively, in Sections 3, 4 and 5. Finally, a brief summary of the published RF and millimeter-waves ICs based on FD SOI technology is presented in Section 6 before concluding.

2. Analogue/RF performances

Devices studied in this work come from 28LP and 28FDSOI processes by ST-Microelectronics. Transistors with gate lengths Lg from 30 to 150 nm are measured. More details on the process can be found in [PLA 12]. The analogue performances of those devices have been presented in details in [MAK 16]. Bulk devices feature a thin SiGe layer for performance enhancement via the improvement of the channel carrier mobility. As demonstrated in [MAK 16], improved control of short channel effects results in much lower subthreshold slope and DIBL in FD SOI comparing with bulk. The off-state current is two orders of magnitude lower in FD SOI confirming that leakage is better controlled in FD SOI as expected. Slightly higher on-state current and maximum transconductance in saturation in bulk can be attributed to strain used to boost mobility.

Better control of short channel effects (including parasitic source-to-drain coupling through the substrate) in FD SOI results in reduced outpout conductance gds by a factor of approximately two compared with bulk. Thanks to the reduction of its output conductance, FD SOI outperforms bulk as illustrated in Figures 2 and 3 for devices with different gate lengths. Figure 2 shows the voltage gain as a function of Lg in bulk and FD SOI. For the longest devices (Lg = 150 nm), the gain at high frequency is ~15 dB higher in FD SOI devices than in bulk. In the shortest devices (Lg = 25 nm), this difference is ~5 dB. Figure 3 compares FD SOI and bulk devices in terms of the analogue figure of merit transconductance gm-voltage gain at 100 kHz and 1 GHz. This figure of merit is widely used to benchmark technologies for analogue applications. It can be seen that FD SOI outperforms bulk even at 1 GHz from the analogue perspective.

The mobility channel booster introduced in the case of bulk transistors translates to a slightly larger value of gm for the shorter devices compared with FD SOI as shown in Figure 3.

28LP and 28FDSOI show a similar value for the current gain cutoff frequency (equation 1) of around 270 GHz despite the fact that higher mobility and thus gate transconductance are measured for bulk MOSFET. The good RF performance of FD SOI transistors is achieved thanks to its lower output conductance as well as lower parasitic capacitances. By applying further device and process optimization in SOI technology, e.g. high-mobility channel to obtain higher gm, even better RF performance is expected.

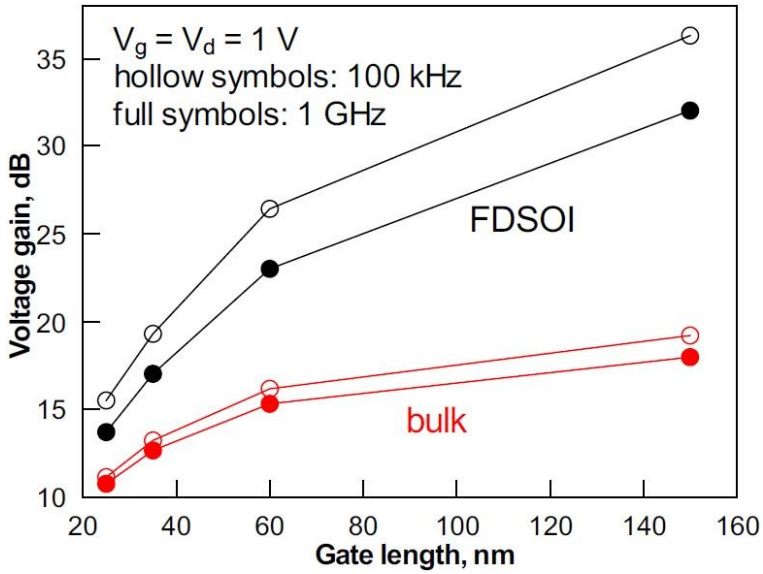


Figure 2. *Voltage gain variation with L_g at 100 kHz and 1 GHz.*

$$f_T \approx \frac{g_m}{2\pi C_{gs}(1 + C_{gd}/C_{gs}) + (R_s + R_d)(C_{gd}/C_{gs}(g_m + g_{ds}) + g_{ds})} \approx \frac{g_m}{2\pi C_{gg}} \quad [1]$$

$$f_{max} \approx \frac{g_m}{4.\pi.C_{gs}(1 + C_{gd}/C_{gs}).\sqrt{g_{ds}(R_g + R_s) + 0.5\,C_{gd}/C_{gs}.(R_s.g_m + C_{gd}/C_{gs})}} \quad [2]$$

where Cgg, Cgs, Cgd, gm, gds, Rs and Rd, are the total gate, the gate-to-source, the gate-to-drain capacitances, the gate transconductance, the channel conductance, and the source and drain parasitic resistances, respectively.

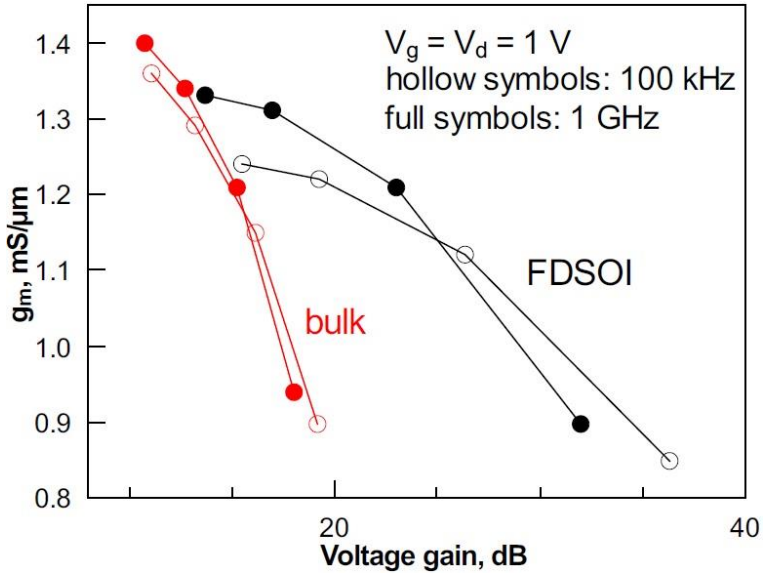


Figure 3. *gm variation with the voltage gain in bulk and FD SOI devices with 25 - 150 nm gate lengths at 100 kHz and 1 GHz.*

ST-Microelectronics optimized their UTBB FD-SOI process in rotating the channel by 45° from the <100> plane and introduced a recessed source-drain (S/D) structure to solve the high source-drain extension access resistances [MD 14, KAZ 16]. The current gain and maximum oscillation cutoff frequencies are presented in Figure 4. Since gm~Wf/Lg and Cgg~Lg.Wf, according to Equation 1, in ideal case fT is expected to increase with length reduction following $1/Lg^2$ and be independent on Wf. Figures 4a and 4b show the fT and fmax variations with Lg and Wf, respectively. fT values for UTBB devices reported in [MD 14] are plotted on the same graph for a sake of comparison. Both fT and fmax

increase with Lg scaling down (Fig. 4a), but fT follows a 1/Lg trend (and an even weaker one in shortest devices) i.e. attenuated comparing with ideally predicted $1/Lg^2$. This is due to velocity saturation, parasitic Rs, Rd and extrinsic Cgg effects. Similar trends were observed in other advanced devices [MD 14]. It is important to point out that in case of devices shorter than 90 nm, fmax becomes lower than fT (Fig. 4a). According to Equation 2, this can be due to the increased of impact of Rg with gate length reduction.

Figure 4b evidences the fT independence on Wf in these devices, whereas in previous work [MD 14] fT dramatically dropped in narrow Wf devices. Wf independence of fT observed for the optimized UTBB fits our expectations thus suggesting that strong parasitic effect at the fingers' perimeter observed in [MD 14] does not appear in studied devices in this Wf range. Furthermore, one can see that Wf reduction leads to increase of fmax (Fig. 4b). This can be a result of the gate resistance reduction in narrow-finger devices. These results evidence that fT and fmax dependences on Lg and Wf deviate from theoretical expectation and being strongly affected by the parasitic elements. To understand the observed trends, complete equivalent circuit elements (both intrinsic and extrinsic, denoted 'i' and 'e') were extracted and analyzed in [KAZ 16]. The main outcomes are the confirmation of the reduction of the source-drain access resistances by at least 30% thanks to the optimized recessed process and also the descrease of the parasitic gate resistance by a factor of 3-4 which explains the strong improvement of fmax.

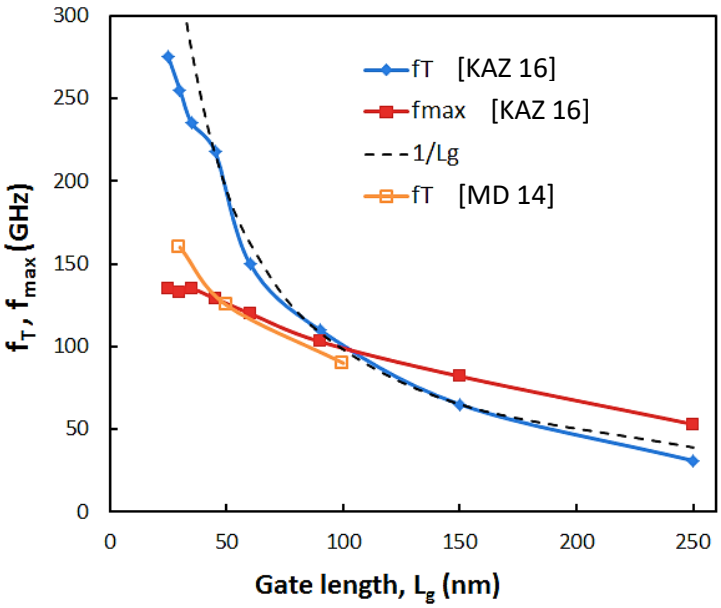


Figure 4a. *fT and fmax versus gate lengths (Lg) for Wf = 2 µm, Nf = 60 [KAZ 16] and Wf = 0.5 µm, Nf = 80 in [MD 14].*

Those experimental results demonstrate clearly that the optimization of the FD SOI process in terms of access parasitic resistances and capacitances is mandatory to take advantage of the improved electrostatic behaviour of the transistors, reduction of SCE, such as the lower output conductance and intrinsic gate-to-drain capacitance in saturation, which could then translate to higher cutoff frequencies.

In [KAZ 17a], a 3-port configuration of FD SOI nMOSFET is employed for extracting the parasitic elements based on an extended small-signal equivalent circuit. The effect of back-gate bias on RF figure of merits (FoMs) for both front and back gates is investigated and discussed through small-signal equivalent circuit elements. Figure 5 illustrates the simplified cross section of the device featuring a particular access to the back-gate, including a heavily doped n-type ground plane (GP) located below the BOX and an n-well which provides a natural substrate insulation between the devices (so called flip-well architecture).

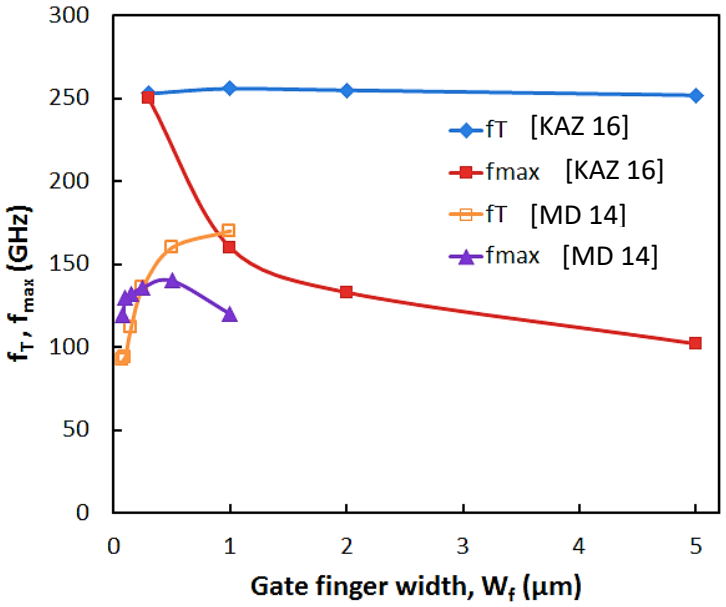


Figure 4b. *fT and fmax versus gate finger widths (Wf) for Lg = 30 nm.*

Figure 6 shows the fT and fmax related to the front-gate as a function of Vgs for Vds = 1 V and back-gate biases, Vbg = 0, 1.8 and 3.0 V. As can be seen in Figures 6a and 6b, at Vbg = 0 V, the maximum fT and fmax for 30 nm-long device is as high as ~355 GHz. The application of a positive Vbg interestingly shifts the maximum cut-off frequencies to a lower Vg, however, with slightly decreased peak values. The consequence of the back-gate biasing is firstly, the possibility to get the fT and fmax peak values at lower Vg, as expected, (due to threshold voltage shift with Vbg) and secondly, flatter fT and fmax vs Vg curves, i.e. wider Vg range with maximum values of fT and fmax. Figure 6a includes results for Vd = 0.6 V. One can see that even at such a low Vd, the device features rather high fT ~280 GHz in a maximum, which is, moreover, stable w.r.t. Vbg (inset in Fig. 6a). Considering low voltage and power applications (< 0.6 V), one can get fT of 280 GHz at Vd =0.6 V as high as fT for Vd=1V by Vbg tuning (example is indicated by arrow in Fig. 6a).

Plots of RF FoMs related to the back-gate transistor fTbg and fmaxbg are illustrated in Figures 7a and 7b versus Vgs showing the double gate behaviour of FD SOI transistor. A maximum fTbg of 55 GHz – 70 GHz and a maximum fmaxbg of 24 GHz – 27 GHz depending on the bias are achieved. These high frequency performances of the back gate electrode open new opportunities of RF design circuits such as an active RF mixer using the top and back gate electrodes for the RF and LO (Local Oscillator) input signals, thus getting the IF (Intermediate Frequency) signal at the transistor output (drain).

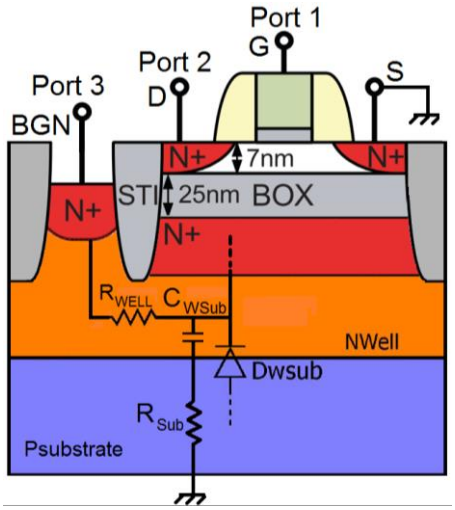


Figure 5. *Simplified cross section of studied FD SOI nMOSFET with back-gate scheme.*

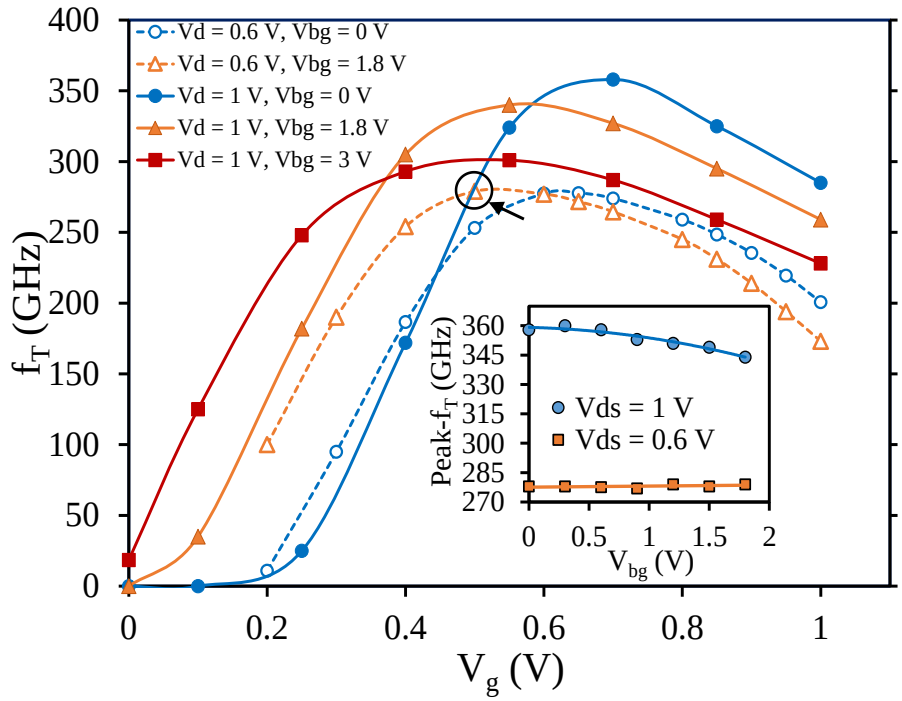


Figure 6a. *Front-gate fT for Vds = 0.6 and 1 V as a function of Vg for various Vbg.*

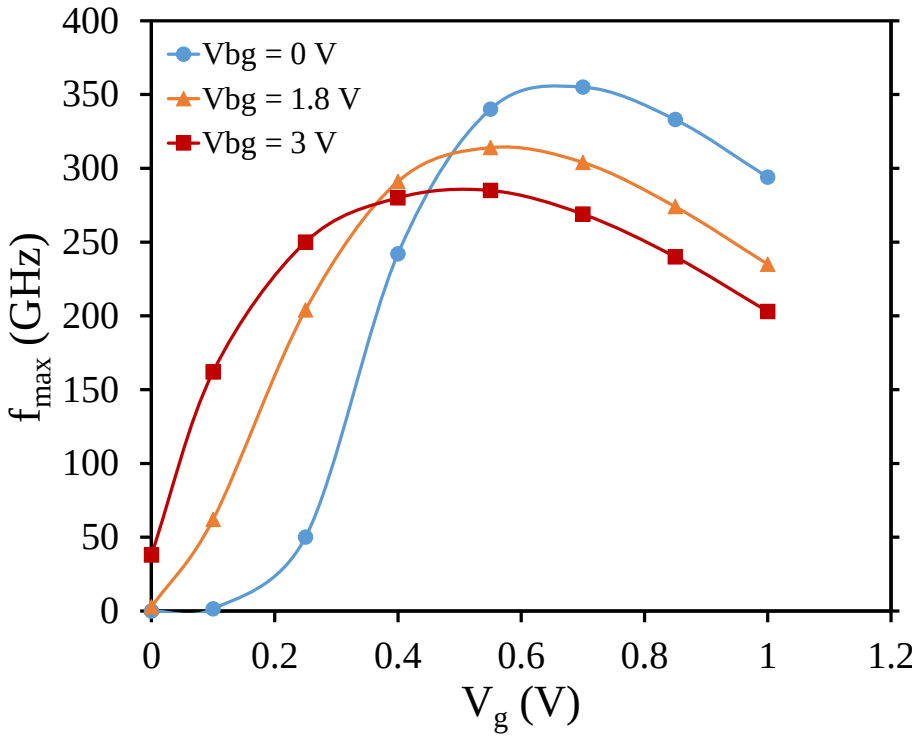


Figure 6b. *Front-gate fmax for Vds = 1 V as a function of Vg for various Vbg.*

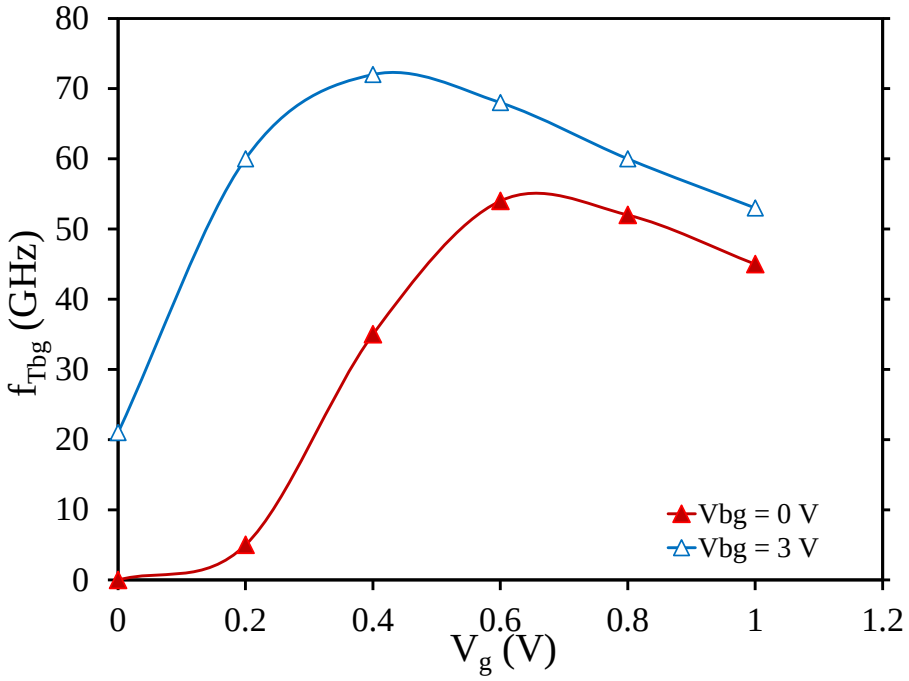


Figure 7a. *Back-gate fTbg vs. Vg for Vbg = 0 and 3 V.*

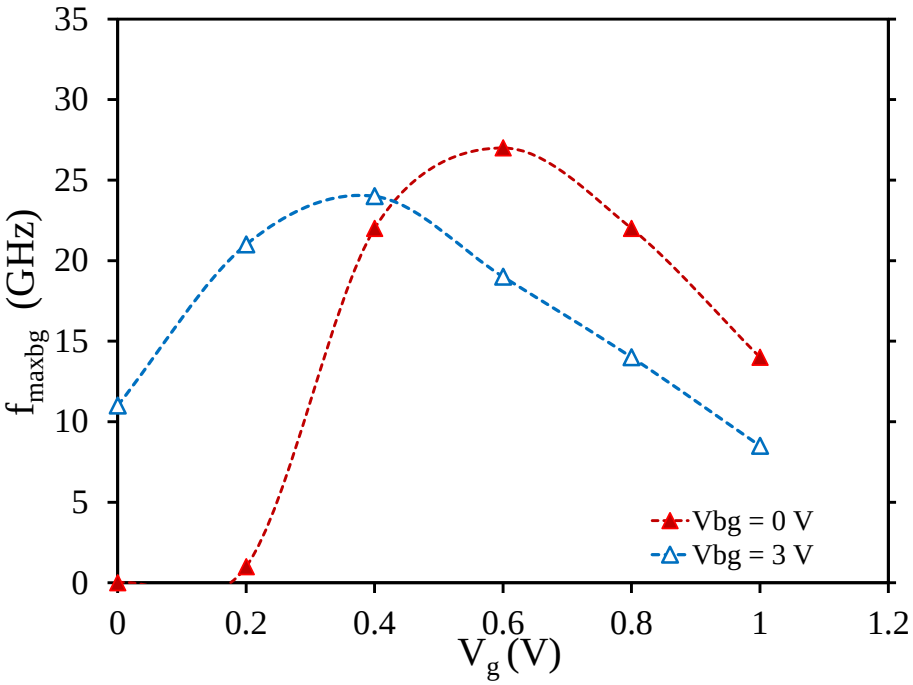


Figure 7b. *Back-gate fmaxbg vs. Vg for Vbg = 0 and 3 V.*

3. Self-heating issue

Self-heating in semiconductor devices arises because of device scaling which naturally leads to higher current and power densities. Self-heating strongly affects analogue device performance. It results in a higher device temperature, which leads to threshold voltage shift, mobility reduction, and consequently degradation of the output current. Self-heating in FD SOI is expected to be aggravated due to thin Si film with poorer thermal properties than Si bulk and by a presence of the buried oxide (BOX) that limits removal of the Joule heat from the device channel to the substrate. However, in a MOSFET several thermal paths exist and their relative importance to heat dissipation is an open scientific question. There are several self-heating characterization techniques published in the literature

to extract those parameters, such as gate resistance [MAU 90], noise thermometry [MEN 16], pulsed I–V [MAK 13], AC conductance [TU 95] and RF extraction [MAK 11] techniques. The parameters which describe the self-heating behaviour of a device are the thermal resistance (Rh) , the thermal capacitance (Cth) and their product (Rth.Cth) which calls the thermal time constant of the device expressed in second. The thermal time constant indicates the time required for the current flow in the transistor channel to respond to a change in its ambient temperature. The thermal resistance is inversely proportional to the device surface area, while the thermal capacitance is proportional to its volume. As MOSFETs are scaled down, their surface to volume ratio increases and thus, their thermal time constant is decreasing. For the most advanced devices it enters to the nanosecond range. Therefore, in order to characterize self-heating using the pulsed I–V method very narrow pulses (ideally a few nanoseconds) are required. Due the limitation of current pulsed I-V equipement, frequency domain method in the GHz range is more suited [MAK 13].

In [MAK 16], the self-heating behaviour of 28LP and 28FDSOI transistors have been measured and compared. It has been experimentally demonstrated that the isothermal frequency for both transistors is around 100 MHz which corresponds to a pulse width of 1.6 ns. Such a short pulse is not achievable with the currently available on-wafer characterization equipment on the market. Thus, the pulsed I–V technique can significantly underestimate self-heating when applied to the most advanced transistors nodes. RF extraction method is then the technique to be used to study the self-heating issue in advanced technological nodes. The thermal resistance Rth was extracted in bulk and FD SOI devices and benchmarked in Figure 8 against experimental data for various technologies [KAR 12, MAK 12, MAK 14b, MAK 14c] as a function of the gate length. The benchmarked technologies are ultra thin body (UTB) and UTBB devices with various BOX thicknesses as well as 28 nm technology node FD SOI and bulk devices. The main features of the compared devices are listed in Table 1. As seen in Figure 8, Rth in bulk devices is lower than in FD SOI of all gate lengths up to 228 nm. This can be attributed to enhanced heat removal from the channel to the substrate in bulk devices compared with FD SOI. In FD SOI, BOX with low thermal conductivity impedes effective heat dissipation. Furthermore, thermal conduction in the thin Si film is two orders of magnitude lower than in bulk Si [MD 14]. Rth in the bulk devices is lower than in any of benchmarked SOI devices. The temperature rise due to self-heating at gate voltage Vg and drain voltage Vd of 1 V is ~32 K in bulk and ~87 K in FD SOI 28 nm devices. Rth dependence on the gate length is weaker in bulk devices than in FD SOI. This can be attributed to the domination of the thermal path through the substrate in bulk devices at all gate lengths. In FD SOI devices, the relative importance of other thermal paths (e.g. through the source and drain) might become more important as the gate length is scaled.

Symbol	Technology	Reference	t_{BOX} (nm)	t_{Si} (nm)
□	UTBB	[KAR 12]	10	8
+	UTBB	[MAK 12]	25	7.5
×	UTBB	[MAK 12]	10	7
○	UTB	[MAK 14b]	145	10
✳	28 nm FD SOI	[MAK 14c]	25	7
△	28 nm FD SOI	[MAK 16]	25	7
△	28 nm bulk	[MAK 16]	-	-

Table 1. *Key parameters of the devices compared in Fig. 8.*

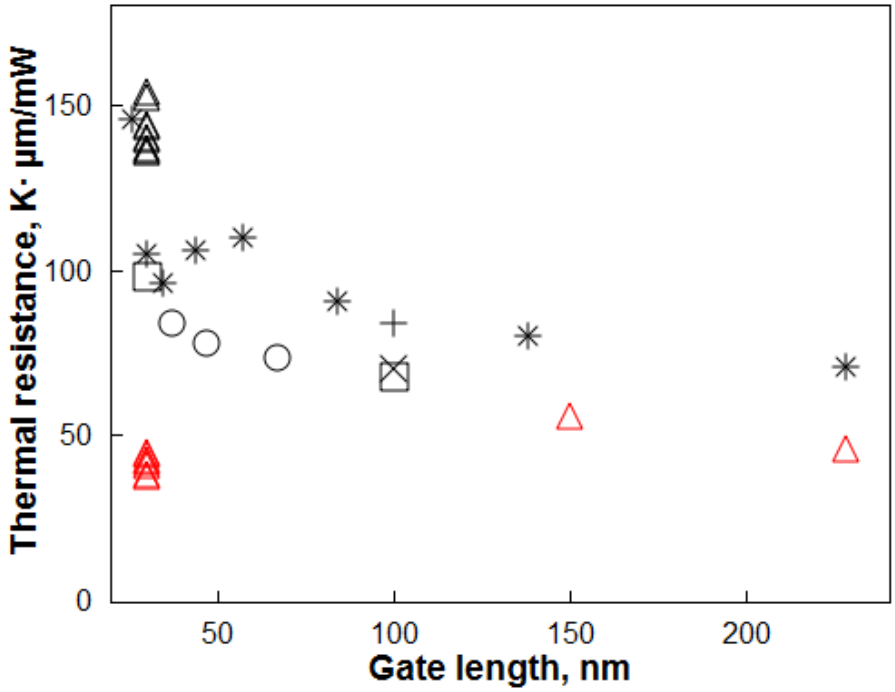


Figure 8. *Thermal resistance in devices of various technologies. Device details are listed in Table 1.*

Figure 8 shows that thanks to the BOX reduction from 25 down to 10 nm the thermal resistance of FD SOI decreases by approximately 35%. It is worth mentioning that despite stronger self-heating than in bulk, FD SOI outperforms bulk technology over a wide frequency range in terms of analogue/RF performance as briefly presented in previous section and in [MAK 16].

4. Non-linear characteristics

Non-linearity is key in telecommunication circuits design. Drain current of any MOSFET features non-linear dependence on applied bias. This is expected to be aggravated in advanced devices with dimensions shrinkage due to short-channel and parasitic effects. Number of effects comes into play complicating non-linearity modeling and making correct non-linear behaviour prediction a complex task.

Figure 9 plots distortion of 2nd and 3rd order, HD2 and HD3, in bulk and FD SOI devices. One can see that there exists a clear bias and current conditions at which FD SOI device outperforms bulk counterpart. It is worth pointing that HD2 is minimized at lower Id and Vg-Vth (not shown) ranges in FD SOI than in bulk devices, thus of interest for further low-power applications [KIL 17].

As presented in Section 2, the high frequency performance of FD SOI transistor can be tuned and enhanced by biasing proprely the back gate electrode. In [KAZ 17b], the non-lienar behaviour of FD SOI has been studied for different back gate bias schemes. Figure 10 shows that HD2 minimum is shifted by Vbg to higher Id (and to lower Vg following Vth (Vbg) trend, not shown due to lack of space). Thus, depending on the regime (bias, current), HD2 can be considerably reduced. This is interesting from a design point of view. If one needs a certain current level, the better linearity can be achieved for that current by changing the Vbg. For example, Figure 10 shows that 10-30 dB improvement can be obtained depending on the Vbg at given normalized current Id/(W/L) > 12 µA.

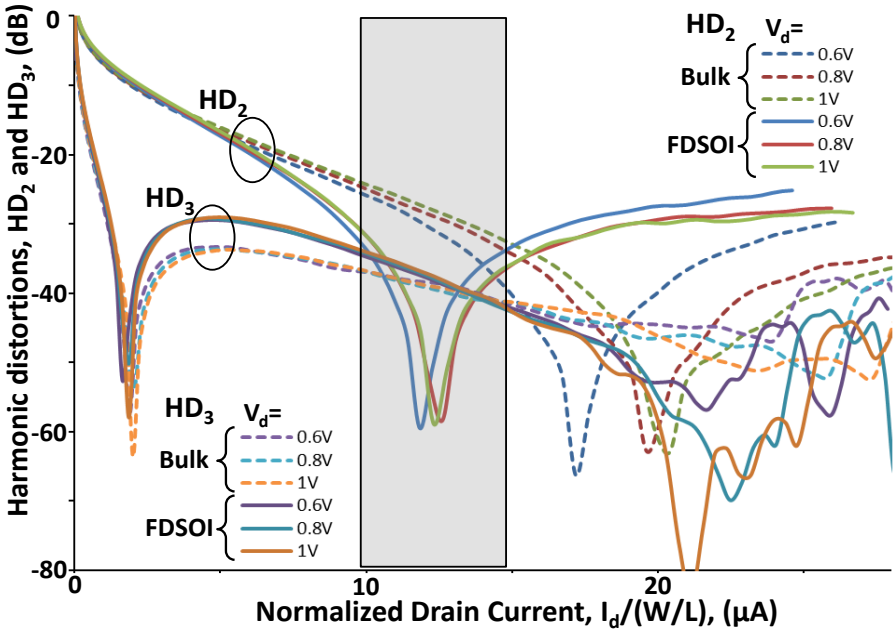


Figure 9. *Experimental harmonic distortions HD2 and HD3 as a function of normalized Id curves for FD SOI (solid lines) and bulk (dashed lines) MOSFETs measured at various Vd. Shaded area gives example of conditions at which FD SOI device outperforms bulk counterpart.*

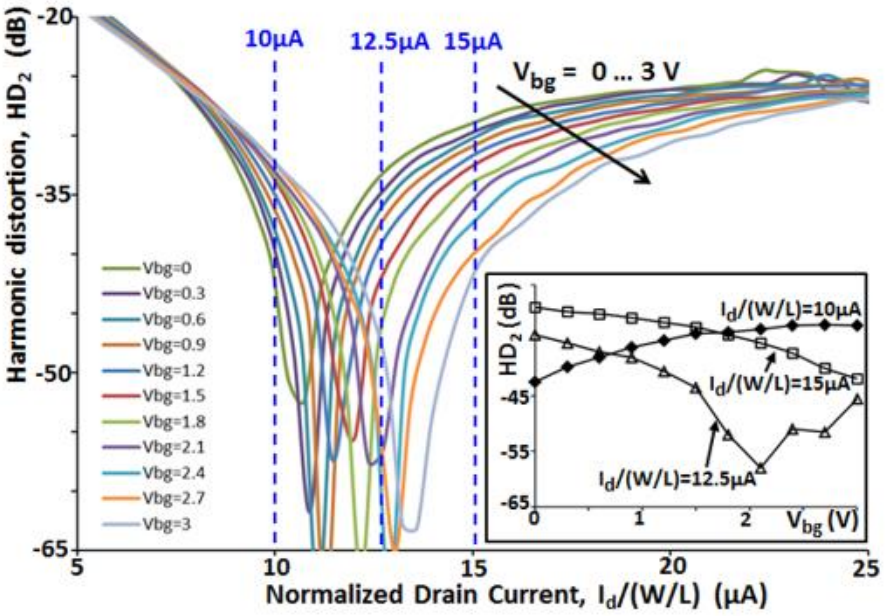


Figure 10. *Experimental HD2-Id curves of FD SOI device at various Vbg. Vd = 1 V. Lg = 30 nm. W = 40 µm. Insert gives HD2 vs. Vbg.*

5. High frequency behaviour at cryogenic temperature

Motivation for the in-depth study of advanced technologies at cryogenic temperatures is two-fold: (i) space applications and (ii) control and read-out circuitry around quantum bits ("qubits") by an integrated control system [BEC 17, BOH 17, BEC 18, KAZ 18a, KAZ 18b]. The co-integration of the qubits and their control system can further reduce the thermal noise by removing the need for direct interconnections from the qubits to a control system operating at room temperature (RT). Thus, in a control system operating at cryogenic temperature, the analogue/RF building blocks (multiplexers, low-noise amplifiers, oscillators etc.) should be designed in cryogenic CMOS electronics. Influence of cryogenic temperature on 28 nm bulk and FD SOI DC characteristics was already addressed with a main focus on EKV model in [BEC 17] and [BEC 18], respectively.

In [KAZ 18a], we investigated the properties of 28 nm FD SOI transistors for cryogenic applications from DC to RF covering electrostatic, analogue and RF figures of merit. We demonstrated strong improvement of transconductance (gm) to drain current (Id) ratio gm/Id, gm, Id, and current gain cut-off frequency (fT) at 77 K. Figure 11 shows fT and fmax as a function of the gate length at 300 K and 77 K for the case of low Vds of 0.6 V. Low voltage operation is indeed of high interest particularly for cryogenic operation where it is crucial to keep the heat dissipation by the device itself as low as possible in order to not alter the ambience cryogenic temperature. One can see that even at Vds = 0.6 V this technology allows for rather high fT ~240 GHz and fmax ~135 GHz in shortest device at 300 K with further improvement up to fT ~323 GHz and fmax ~150 GHz at 77 K proving the advantage of this technology for low-voltage cryogenic circuits.

In [KAZ 18b], the complete small-signal equivalent circuit of measured FD SOI transistors was extracted over a wide temperature range down to 77 K. Figure 12a shows the extracted intrinsic and extrinsic gate transconductance versus the channel length at 300 and 77 K, while Figure 12b presents the extracted gate and total source/drain parasitic resistances. We clearly observe the nice increase of the gate transconductance with the temperature drop thanks to mainly the carrier mobility increase at lower temperature. Figure 12b illustres the huge increase of the gate resistance for shorter transistor explaining the moderate improvement of fmax with the transistor channel shrinkage (Fig. 11), and the very weak impact of temperature on the extracted resistance values. The weak temperature dependence Rsd and Rg can be explained by the behaviour of its different components, e.g. source/drain highly-doped regions, metallic interconnection lines and vias which all these elements are known to show only a very small reduction of resistance at low temperature [NOR 78]. As a result of very slight Rsd variation with temperature, Figure 12a shows almost constant difference between gme and gmi for each device from 300 K down to 77 K. The effect of Rsd itself in shorter devices and at lower temperature (i.e. the cases featuring higher gmi level) is more pronounced, as can be seen from stronger difference between their gmi and gme. Similar analyses (not shown here) have been conducted in [KAZ 18b] on the capacitive elements of the measured FD SOI transistors and it has been demonstrated that the gate capacitances as well as the output conductance do not change much with temperature lowering and therefore, fT and fmax temperature-dependencies are mostly related to gm (due to carrier mobility and Rsd) temperature-dependence.

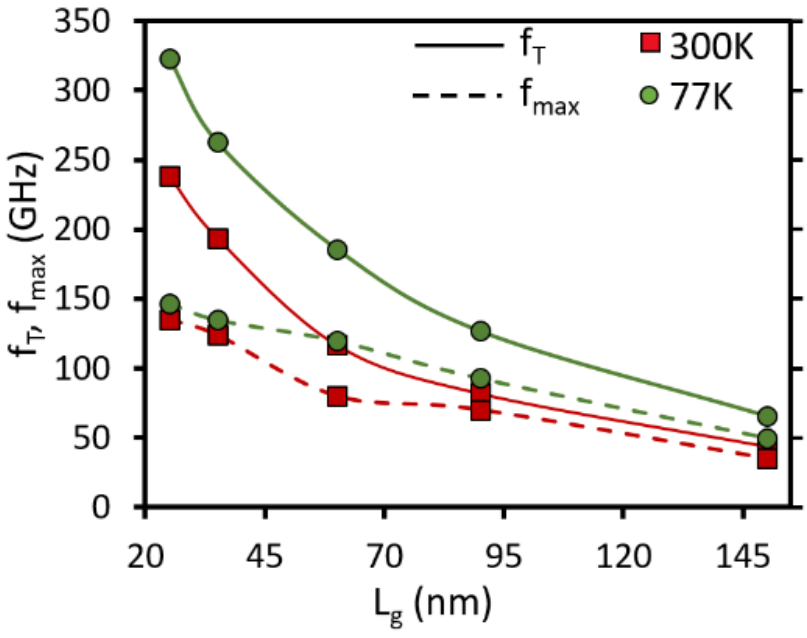
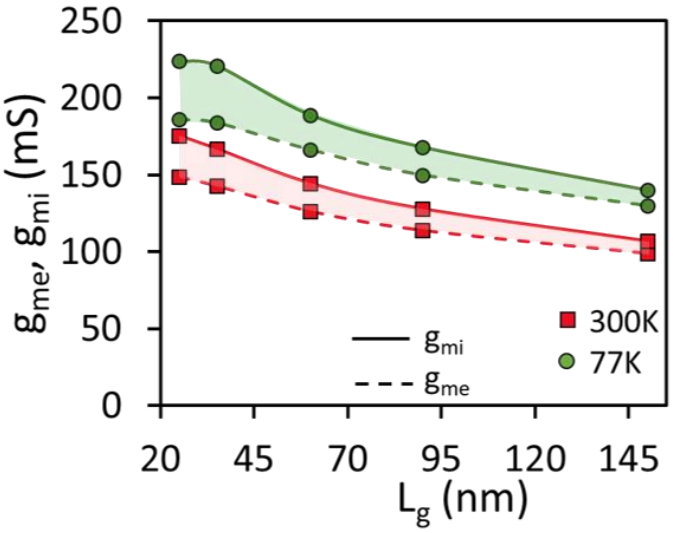
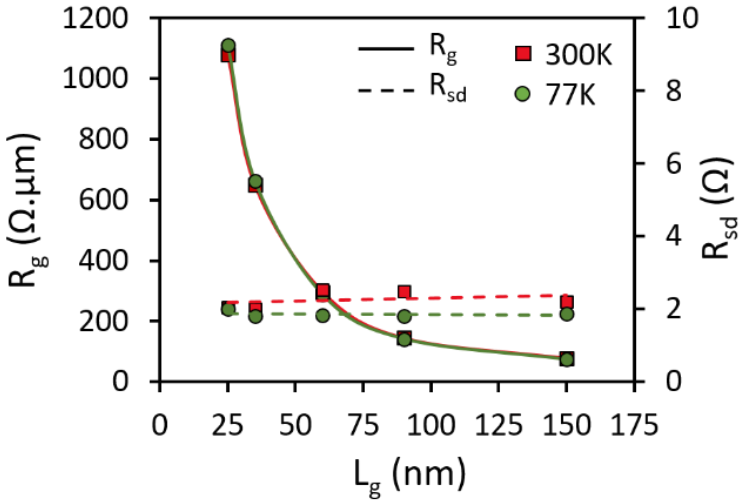


Figure 11. *fT and fmax vs. Lg for 77 K and 300 K in saturation at low-Vds (Vds = 0.6 V) and at Vgs that corresponds to maximum gm.*



(a)



(b)

Figure 12. *(a) Maximum gmi, gme vs. Lg at 77 K and 300 K for Lg = 25, 60 and 150 nm in saturation (Vds = 1 V) and at Vgs that corresponds to maximum gm, (b) Rg, Rsd vs. Lg at 77 K and 300 K vs. Lg extracted with Bracale method [BRA 00].*

6. FD SOI RF and millimeterwaves ICs

These recent years we can observe a growing interest for applications in W-band regime such as mm-wave imaging, radar transceivers, internet of things (IoT) applications, as well as short-distance high data-rate communications including the 5G standard. Traditionally, the III-V semiconductor technologies have been preferred for such systems, due to their superior power gain and noise performance compared with their silicon counterparts. However, based on the quite encouraging reported performance of the FD SOI transistors at RF and millimeterwaves, several researchers designed front-end module blocks such as Low Noise Amplifiers (LNAs) [ZAI 18, UL 18, KAR 17, VAH 16, LUO 15] and Power Amplifiers (PAs) [LAR 15, MOR 17] those last years. Table 2 summarizes the main published figures of merit of LNAs based on FD SOI technology. The great benefit of FD SOI technology is clearly its very low power consumption and its design active area which is significantly smaller (not presented here).

In [LAR 15], A. Larie *et al*. introduces a novel PA technique to relax the tradeoff between Pdc and P1dB, achieving a P1dB of 18.2 dBm with 21% PAE at P1dB drawing a mere 74 mW Pdc from its 1 V power supply. Contrary to the Doherty architecture which combines two PA Classes to improve P1dB, with limited flexibility and area overhead, they achieve linearization at device level, as segmented

parallel transistors operate in different Classes using the UTBB FD-SOI back gate for threshold voltage adjustment. This reconfigurable solution does not alter the RF path and effectively linearizes the PA while consumption dynamically tracks RF power. In [MOR 17], A 28 GHz self-contained power amplifier is designed using the 28 nm FD-SOI CMOS technology from STMicroelectronics taking advantage of the back gate for threshold voltage adjustment. It is based on a balanced topology which offers load-variation insensitivity, enhances stability, and improves input and output matching. The use of integrated planar hybrid coupler allows a compact and an efficient design. The proposed balanced PA demonstrates the potential of a VSWR robust PA for 5G phased array applications.

Further improvement of the FD SOI technology for RF and mm-wave regime could come in the near future with the move from standard resistivity SOI substrate to high-resistivity or trap-rich SOI substrates [RAS 16], which would lead to passive elements and matching networks with better quality factor as well as reduced insertion loss along transmission lines and lower crosstalk between circuits blocks.

References	Gain (dB)	Frequency (GHz)	Noise Figure (dB)	IIP3 (dB)	Pdc (mW)	Supply voltage (V)	Techno
[ZAI 18]	16.8	0.45-6	7.3	-16	0.3	0.6	28 nm
[UL 18]	15	0.7-2.7	5.1	+14	11.5	1	28 nm
[KAR 17]	12	53-117	6		38.2		28 nm
[VAH 16]	13.8	90	8		37.5	1	28 nm
[LUO 15]	11	6	3.6-4.9		81-209	2	32 nm

Table 2. *FD SOI LNAs figures of merit.*

7. Conclusion

RF SOI continues to grow at 20% Compound Annual Growth Rate, driven by switch, power amplifier, low noise amplifier, etc. Present ramping of 300 mm wafers is enabling nodes below 65 nm, targeting 5G, millimeter-waves, and advanced System-on-Chip. The mainstream RF SOI technology today is still partially depleted. The success of this technology comes from the great combination between the low power with well controlled short channel effects transistors and the high quality (highly-resistive) trap-rich SOI substrate. The next innovative step will be the integration of fully depleted SOI transistors with the most advanced silicon-based substrate such as the trap-rich to come up with very competitive solutions compared with III-V technologies which are still the major drivers for mm-wave applications.

8. Acknowledgement

All the results presented in this invited paper have been obtained with the active participation of my colleagues Prof. D. Flandre, Dr. V. Kilchytska, Dr. M. K. Md Arshad, Dr. S. Makovejev, Mr. B. Kazemi Esfeh, Mr. M. Rack, Mr. L. Nyssens and Mr. M. Nabet. I would like to thank all of them for their precious work and the inspiring discussions we have together on the topic of RF SOI. I would like also to thank the teams of ST-Microlectronics and CEA-Leti for providing us with state-of-the-art MOSFETs and SOITEC for our successful collaboration on the trap-rich SOI substrate.

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